# D8555N

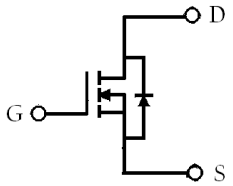
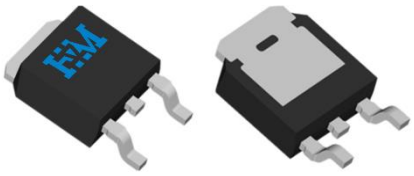
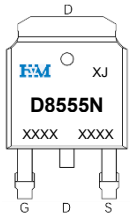
| | | | |
|---|---|---|---|
| $BV_{DSS}$ | **30** | | V |
| $I_D$@$V_{GS}$=10V, $T_C$=25°C | **85** | | A |
| $R_{DSON}$, $T_C$=25°C | Typ | Max | |
| @$V_{GS}$=10V, $I_D$=30A | **4.5** | **5.5** | mΩ |
| @$V_{GS}$=4.5V, $I_D$=20A | **5.5** | **7.0** | |

***100% $\Delta V_{ds}$ TESTED!***

***100% UIS TESTED!***

## Features

- Super Low Gate Charge
- Green Device Available
- Excellent CdV/dt effect decline
- Advanced Trench technology

| Equivalent Circuit | TO-252 | Marking & Pin Assignment |
|---|---|---|
|  |  |  |





**Package Marking and Ordering Information**

| Device Name | Marking | Device Package | Quantity |
|---|---|---|---|
| HMD8555N | D8555N | TO-252 | 2500/Reel |

**Table 1. Absolute Maximum Ratings (TA=25℃)**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain-Source Voltage ($V_{GS}$=0V) | 30 | V |
| $V_{GS}$ | Gate-Source Voltage ($V_{DS}$=0V) | ±20 | V |
| $I_{D\ (DC)}$ | Drain Current-Continuous (Tc =25℃) [1] | 85 | A |
| | Drain Current-Continuous (Tc =100℃) [1] | 58.5 | A |
| $I_{DM\ (pulse)}$ | Drain Current-Continuous@ Current-Pulsed [2] | 340 | A |
| $P_D$ | Maximum Power Dissipation (Tc=25℃) [4] | 81 | W |
| $E_{AS}$ | Single Pulse Avalanche Energy [3] | 225 | mJ |
| $T_J$, $T_{STG}$ | Operating Junction and Storage Temperature Range | -55 To 150 | ℃ |

**Table 2. Thermal Characteristic**

| Symbol | Parameter | Max | Unit |
|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance Junction-Case [1] | 1.85 | ℃/W |

**Table 3. Electrical Characteristics (TA=25℃unless otherwise noted)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **On/Off States** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$=0V $I_D$=250μA | 30 | | | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current(Tc=25℃) | $V_{DS}$=30V, $V_{GS}$=0V | | | 1 | μA |
| $I_{GSS}$ | Gate-Body Leakage Current | $V_{GS}$=±20V, $V_{DS}$=0V | | | ±100 | nA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$=$V_{GS}$, $I_D$=250μA | 1.0 | 1.5 | 2.5 | V |
| $R_{DS(ON)}$ | Drain-Source On-State Resistance [2] | $V_{GS}$=10V, $I_D$=30A | | 4.5 | 5.5 | mΩ |
| | | $V_{GS}$=4.5V, $I_D$=20A | | 5.5 | 7.0 | mΩ |
| **Dynamic Characteristics** | | | | | | |
| $R_G$ | Gate Resistance | $V_{DS}$=0V, $V_{GS}$=0V f=1.0MHz | | 2.0 | | Ω |
| $C_{iss}$ | Input Capacitance | $V_{DS}$=15V, $V_{GS}$=0V f=1.0MHz | | 2230 | | PF |
| $C_{oss}$ | Output Capacitance | | | 300 | | PF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 275 | | PF |
| **Switching Times** | | | | | | |
| $t_{d(on)}$ | Turn-on Delay Time | $V_{DS}$=15V, $V_{GS}$=10V, $I_D$=20A, $R_G$=2.0Ω | | 7.0 | | nS |
| $t_r$ | Turn-on Rise Time | | | 14.0 | | nS |
| $t_{d(off)}$ | Turn-Off Delay Time | | | 35.0 | | nS |
| $t_f$ | Turn-Off Fall Time | | | 12.0 | | nS |
| $Q_g$ | Total Gate Charge | $V_{DS}$=15V, $V_{GS}$=10V, $I_D$=20A | | 42.5 | | nC |
| $Q_{gs}$ | Gate-Source Charge | | | 7.0 | | nC |
| $Q_{gd}$ | Gate-Drain Charge | | | 12.0 | | nC |
| **Source-Drain Diode Characteristics** | | | | | | |
| $I_{SD}$ | Source-Drain Current (Body Diode)[1.5] | | | | 85 | A |
| $V_{SD}$ | Forward On Voltage [2] | $I_{SD}$=20A, $V_{GS}$=0V, $T_J$=25℃ | | | 1.2 | V |
| $t_{rr}$ | Reverse Recovery Time | $T_J$=25℃ $I_F$=20A, di/dt=100A/μs | | 14 | | nS |
| $Q_{rr}$ | Reverse Recovery Charge | | | 5 | | nC |
| $t_{on}$ | Forward Turn-on Time | Intrinsic turn-on time is negligible (turn-on is dominated by LS +LD) | | | | |

## Notes:

1.The data tested by surface mounted on a 1 inch$^2$ FR-4 board with 2OZ copper.

2.The data tested by pulsed , pulse width≦300us , duty cycle≦2%.

3. The test condition is $V_{DD}$ =20V, $V_{GS}$ =10V, L=0.5mH, $I_{AS}$=30A.

4.The power dissipation is limited by 175℃ junction temperature.

5.The data is theoretically the same as $I_D$ and $I_{DM}$, in real applications, should be limited by total power dissipation.

# Typical Characteristics

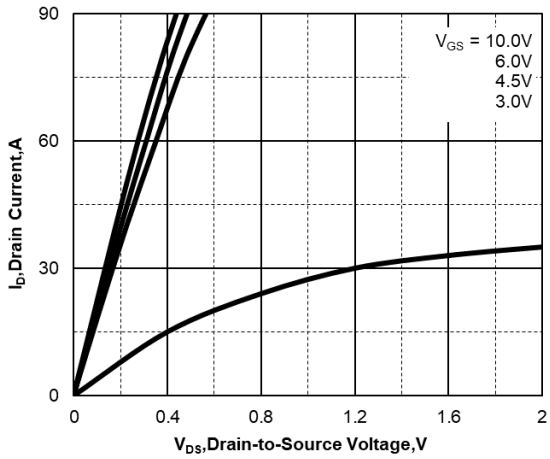



**Fig1: Typical Output Characteristics**

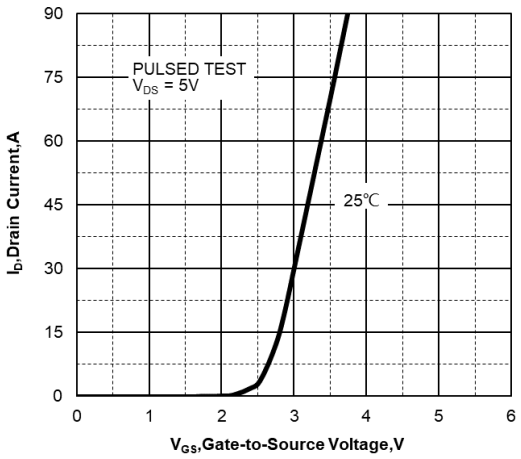



**Fig 2: Typical Transfer Characteristics**

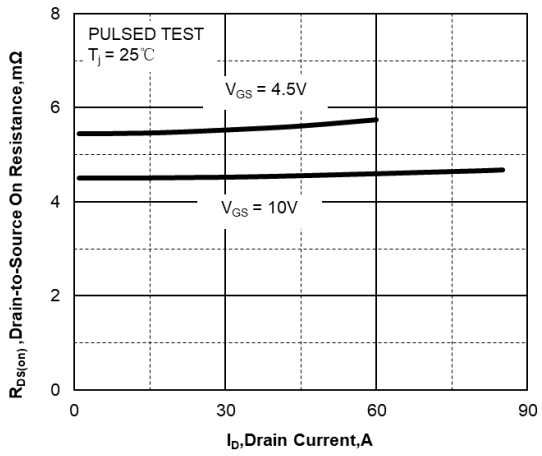



**Fig 3: On-Resistance VS. Drain Current**

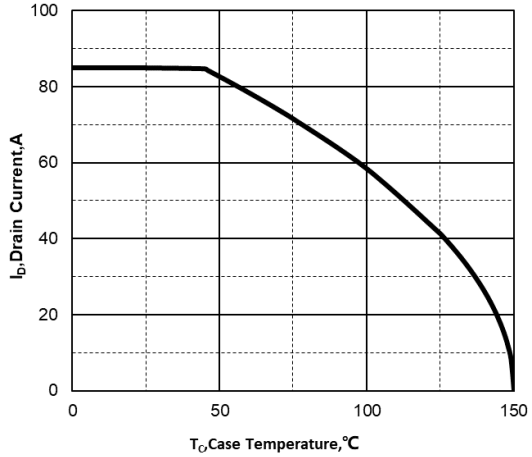



**Fig 4: Maximum Continuous Drain Current VS. Case Temperature**

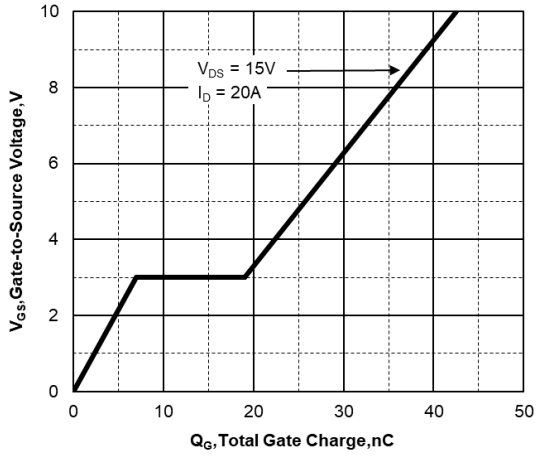



**Fig 5: Gate Charge Characteristics**

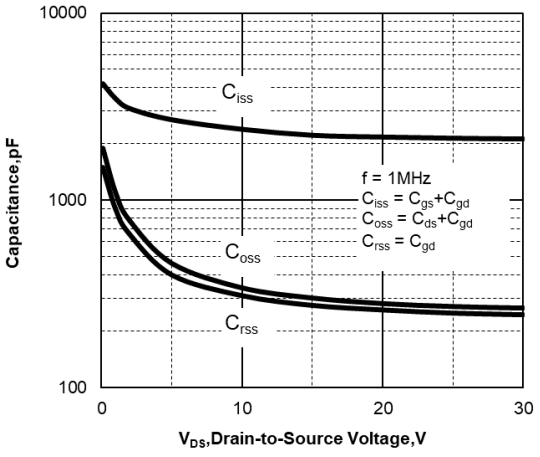



**Fig 6: Capacitance Characteristics**

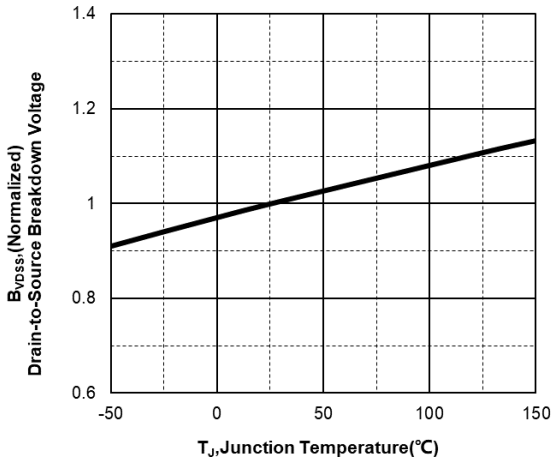



Fig 7: Normalized Breakdown Voltage VS. Junction Temperature

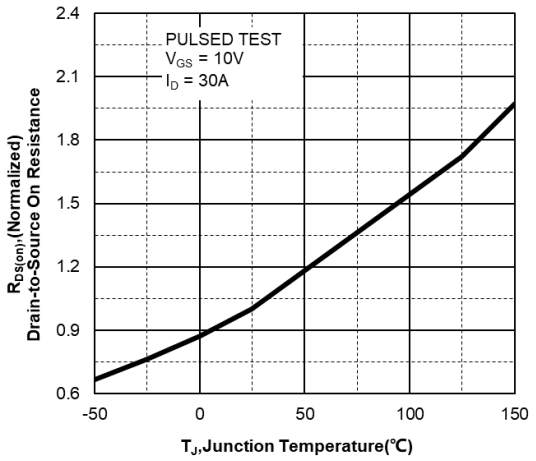



Fig 8: Normalized on Resistance VS. Junction Temperature

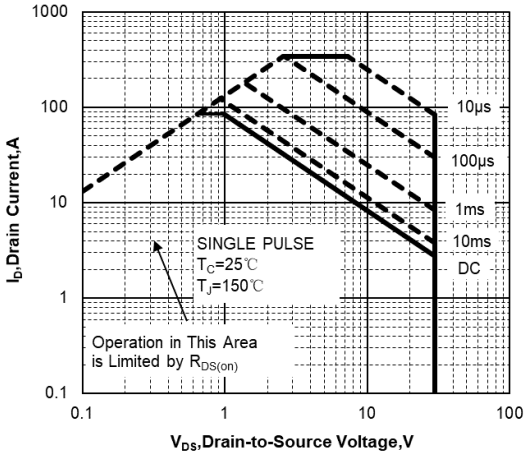



Fig 9: Maximum Safe Operating Area

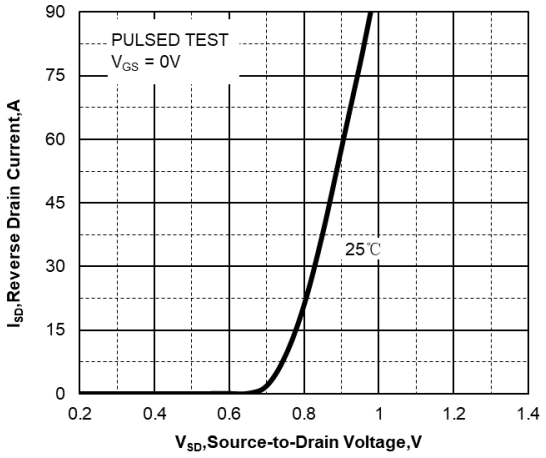



Fig 10: Body Diode Forward Characteristics

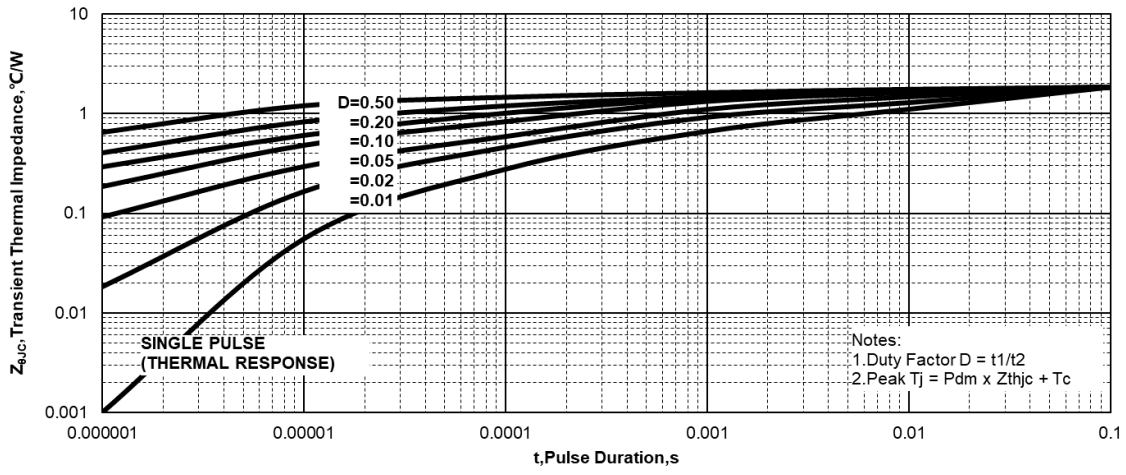



Fig.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case

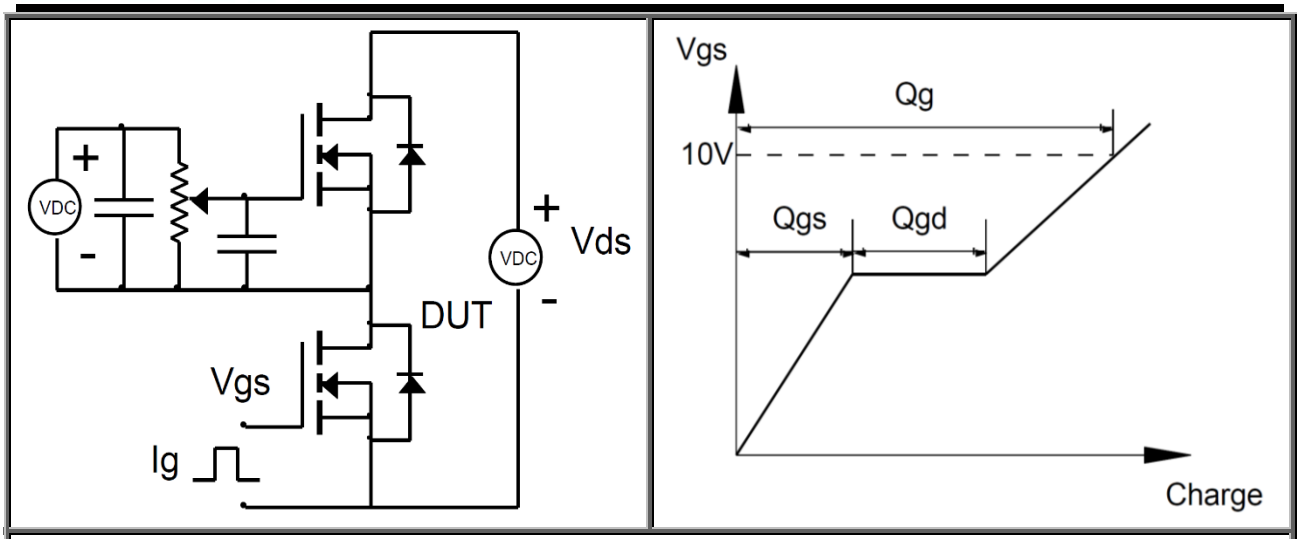



**Fig 12: Gate Charge Test Circuit and Waveforms**

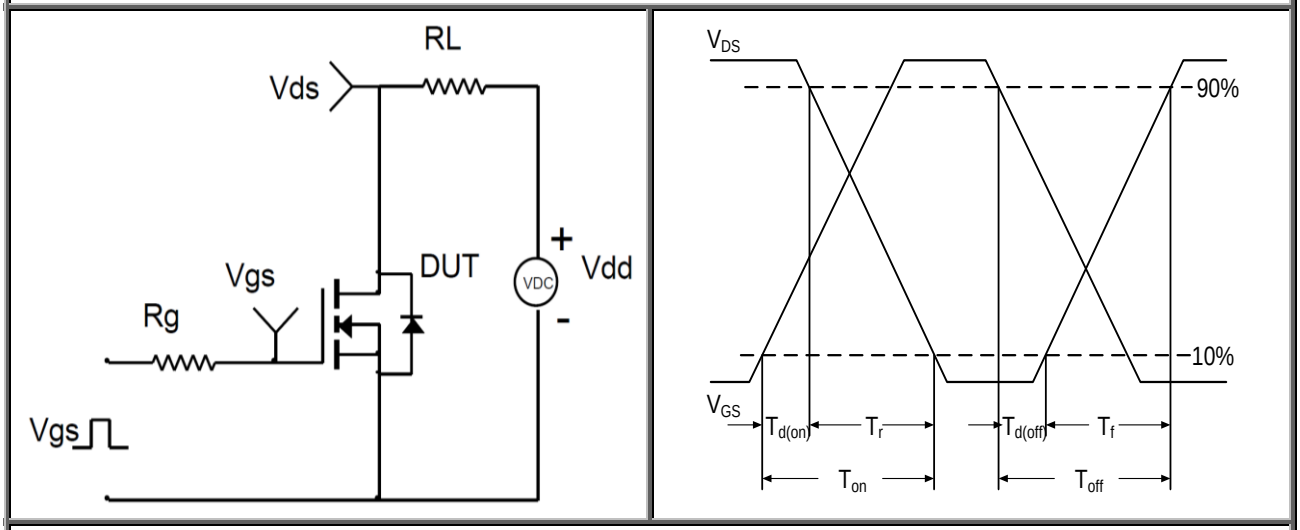



**Fig 13: Resistive Switching Test Circuit and Waveforms**

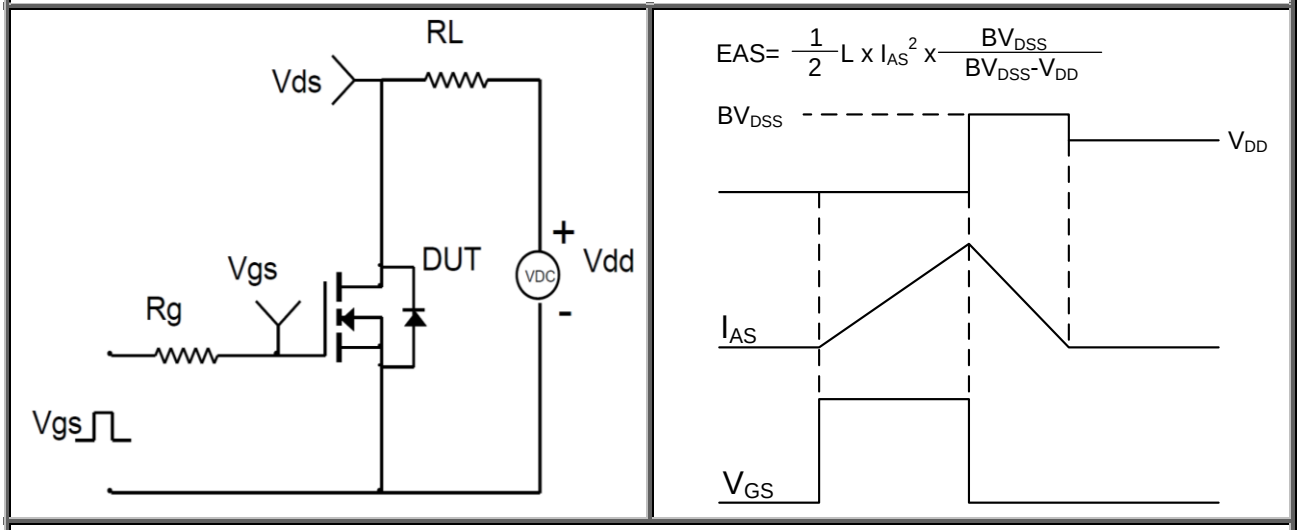
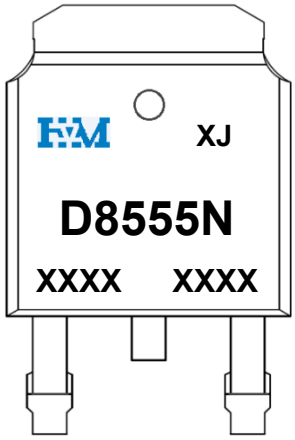


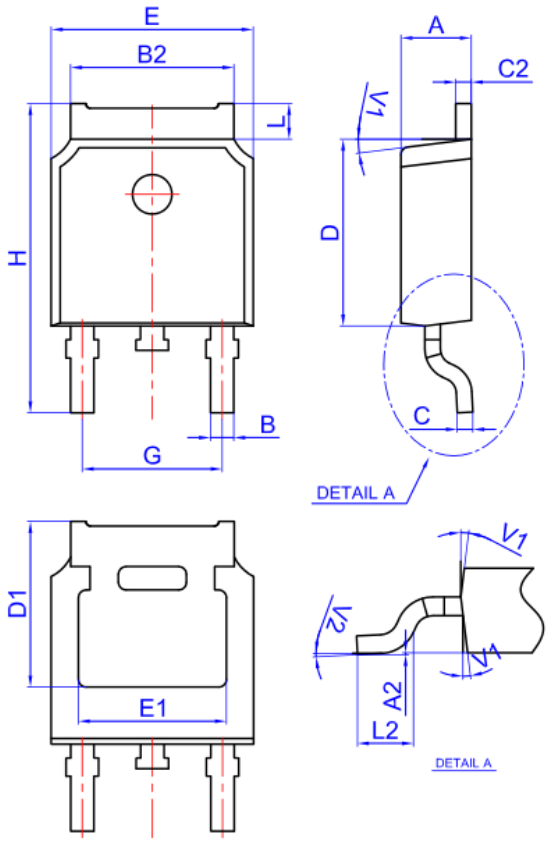

**Fig 14: Unclamped Inductive Switching Test Circuit and Waveforms**

## Marking Information




1st line： HM Logo（left） Coding（right）Changed with Machine Table
2nd line： Device Package and Part Number and Channel and Version
3rd line： Lot number And Date code（XXXX XXXX）
① XXXX： Wafer Lot Number Code Changed with Lot Number
② XXXX： Date code changed with Date Number，Factory Number

# TO-252 Dimension




| Ref. | Dimensions | | | | | |
|---|---|---|---|---|---|---|
| | Millimeters | | | Inches | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 2.10 | | 2.50 | 0.083 | | 0.098 |
| A2 | 0 | | 0.10 | 0 | | 0.004 |
| B | 0.66 | | 0.86 | 0.026 | | 0.034 |
| B2 | 5.18 | | 5.48 | 0.202 | | 0.216 |
| C | 0.40 | | 0.60 | 0.016 | | 0.024 |
| C2 | 0.44 | | 0.58 | 0.017 | | 0.023 |
| D | 5.90 | | 6.30 | 0.232 | | 0.248 |
| D1 | 5.30REF | | | 0.209REF | | |
| E | 6.40 | | 6.80 | 0.252 | | 0.268 |
| E1 | 4.63 | | | 0.182 | | |
| G | 4.47 | | 4.67 | 0.176 | | 0.184 |
| H | 9.50 | | 10.70 | 0.374 | | 0.421 |
| L | 1.09 | | 1.21 | 0.043 | | 0.048 |
| L2 | 1.35 | | 1.65 | 0.053 | | 0.065 |
| V1 | | 7° | | | 7° | |
| V2 | 0° | | 6° | 0° | | 6° |

# Disclaimer

**All product specifications and data are subject to change without notice.**

**For documents and material available from this datasheet, Suzhou HuaMeiYiXin does not warrant or assume any legal liability or responsibility for the accuracy, completeness of any product or technology disclosed hereunder.**

**No license, express or implied, by estoppels or otherwise, to any intellectual property rights is granted by this document or by any conduct of Suzhou HuaMeiYiXin.**

**The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications unless. Customers using or selling Suzhou HuaMeiYiXin products not expressly indicated for use in such applications do so entirely at their own risk and agree to fully indemnify Suzhou HuaMeiYiXin for any damages arising or resulting from such use or sale.**

**Suzhou HuaMeiYiXin disclaims any and all liability arising out of the use or application of any product described herein or of any information provided herein to the maximum extent permitted by law. The product specifications do not expand or otherwise modify Suzhou HuaMeiYiXin's terms and conditions of purchase, including but not limited to the warranty expressed therein, which apply to these products.**

**Suzhou HuaMeiYiXin Semiconductor CO., Ltd. strives to supply high-quality high-reliability products. However, any and all semiconductor products fail with some probability. It is possible that these probabilistic failures could give rise to accidents or events that could endanger human lives that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.**

**In the event that any or all Suzhou HuaMeiYiXin products (including technical data, services) described or contained herein are controlled under any of applicable local export control laws and regulations, such products must not be exported without obtaining the export license from the authorities concerned in accordance with the above law.**

**Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. Suzhou HuaMeiYiXin believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.**